50 Years of RF and Microwave Sampling

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***Abstract*—Measurement of microwave and UHF signals is often done with sampling techniques. In this paper, the techniques and technology of sampling of electrical signals is reviewed from 1950 to the present. It includes both references to the open literature, as well as an extensive review of relevant patents. It also provides an overview of sampling applications and the use of computer technology to compensate and correct for errors in the sampling process.**

***Index Terms*—Microwave instrumentation and measurement, network analysis, oscilloscopes, RF sampling, samplers, sampling oscilloscopes.**

I. Introduction

THIS PAPER places the improvement in sampling technology in context with the circuits used by RF samplers in RF and microwave instrumentation. This paper emphasizes electronic (as opposed to photonic or electrooptical) sampling. Sampling oscilloscopes are a particular focus.

Sampling systems were originally developed to overcome frequency limitations of electronic instrumentation. The fundamental principal of sampling is the repeated quasi-instantaneous capture of a time-varying waveform by a sampling *gate*. The gate is open and closed by a narrow pulse, which is triggered repeatedly by a time base. This paper will examine the design of sampling gates, time bases, and other aspects.

The time line of sampling instrumentation can be (arbitrarily) divided into four sections: early instruments before the creation of commercial instrumentation, the early commercial era beginning with the Lumatron models, technological improvements due to semiconductor technology, and finally, the sophisticated use of sampling in modern instruments following the introduction of monolithic samplers and digital processing.

A. Post-War Prototypes

The post-war publication of Janssen's (Philips) oscilloscope design [1], [2] is often cited as the first modern sampling instrument. In his two papers, Janssen described in great detail the design and implementation of an instrument capable of sampling waveforms to 30 MHz. The input sampling gate was a EF-50 pentode with the input signal applied to a control grid and the strobe applied to the anode. The pulse generator was a 100-kHz multivibrator differentiated by a passive network.

McQueen [3], [4] described a remarkable sampling oscilloscope (good to 300 MHz) that featured a pentode input gate in a probe. By moving the input gate to the probe, the connecting cable to the test circuit could be eliminated and subsequent measurement distortion greatly reduced. A 500-ps "pre-pulse" (trigger) was externally provided. A "anti-jitter" unit used the time difference between the gate pulse and the "locking pulse" to control the position on the screen. The use of a time interval presages the introduction of "random sampling" (see Section II-F.2). As shown in Fig. 1, this oscilloscope was about the size of a refrigerator. This instrument also used a shorted transmission line in the pulse generator; this concept was developed further by Magelby and Grove [5] for the HP 185A (see Section II-A).

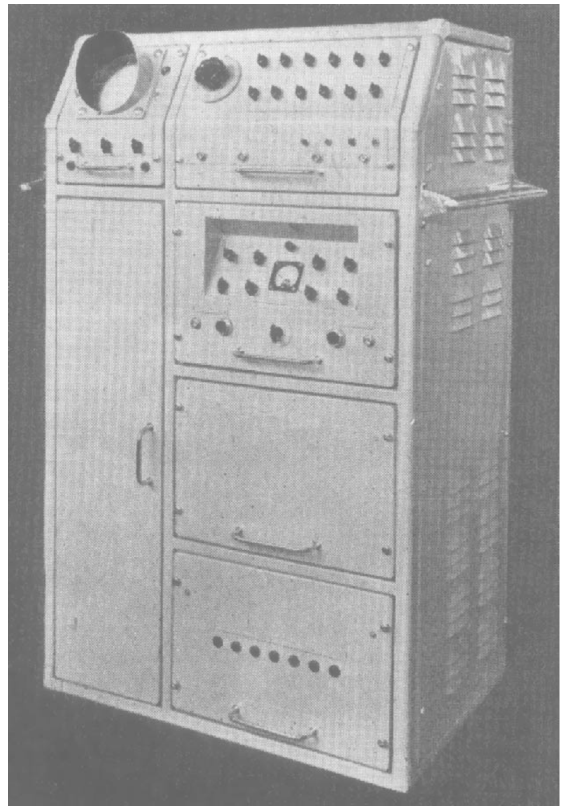

Fig. 1. McQueen's sampling oscilloscope [3] (Republished with permission, CMP Media LLC, Manhasset, NY).

Sugarman's oscilloscope [6], [7] was noteworthy for the following three reasons:

1) use of a semiconductor diode (a Philco Ge 1N263) as the sampling gate (earlier attempts to use planar triodes as a sampling gate were unsuccessful due to the frequency response of the tube);
2) use of a coax delay line (56 ft, 17 m) to delay the signal 82 ns before sampling it, thereby providing an internal trigger;
3) introduction of a second holding capacitor called the "stretcher."

Manuscript received June 10, 2001; revised January 18, 2002.

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Digital Object Identifier 10.1109/TMTT.2002.806934

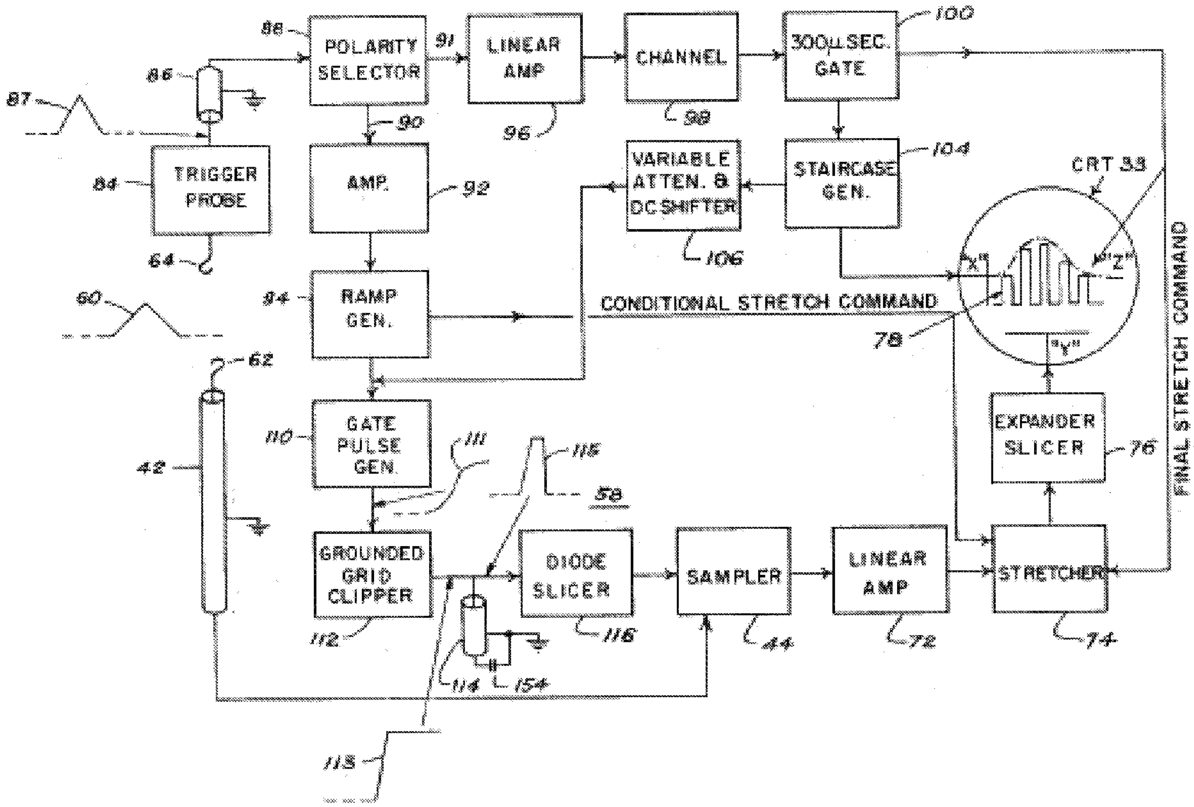


Fig. 2. Sugarman's sampling oscilloscope (figure from the patent [7]).

The "stretcher" was a sample and hold that held the charge until the next sample. The strobe was 500 ps and was generated by differentiating a 7-ns step (in this case, the stretcher hold time was 300 μs). The block diagram is shown in Fig. 2. Sugarman's oscilloscope can be seen as the foundation for all modern sampling oscilloscopes.

Simultaneously, and across the Atlantic, Chaplin [8] described the first transistorized sampling oscilloscope. They used avalanche mode [9], [10] to generate fast gating pulses (1.0 ns) for the sampling gate, time base, and trigger. The sampling gate was a Philco surface barrier SB100 transistor with the pulse generator driving the base. The construction of the sampling gate was also novel: the pulse generator was placed on the opposite side of the sampling gate in a separate probe to shorten the delay from the trigger to the gate.

Amodei [11] (RCA) combined Sugarman's basic instrument (Fig. 2) with the avalanche mode described just two years before by Chaplin [9], [10]. The sampling pulses were 400-ps wide and the venerable 1N23E was used as the sampling gate.

Farber [12] described what must be considered a real-time sampler: the input signal was assumed to have a high-speed repetition rate (approximately 30 MHz) and, therefore, eliminated both the need for a precise trigger and the accompanying delay line. A phase-shift control enabled the operator to vary the location of the pulse on the screen. The sampling pulse was a differentiated squared sine, fed to the "coincidence detector" (sampling diode, a 1N263) in a waveguide.

Bell Laboratories built an experimental sampling oscilloscope [13] with the notable achievement of fabricating a point contact GaAs diode [14] for use as the gate diode; the −6-dB point was 5.5 GHz. They were unable to test the full performance of the instrument (which was calculated to 100 ps) because they lacked a sufficiently fast pulse generator.

In 1960, IBM described an experimental oscilloscope [15]. The sampling gate was an IN21B with stray capacitance as the hold capacitor. It was good to 350 ns.

All of these early instruments were more concerned with increasing the frequency range through the introduction of faster gates and strobing pulses than they were about issues of sampling efficiency or sophisticated time bases. The introduction of commercial instruments would change this emphasis.

II. Commercial Introduction: From 1959

The Lumatron model 112 sampling oscilloscope [16] was the earliest commercial instrument. The design was clearly derived from Sugarman including the use of the 1N263 as the gate. A 85-ns delay line was used before the input to derive the trigger. A 500-ps pulse was used to strobe the gate diode and advance the staircase generator for the horizontal deflection. The follow-on instrument from Lumatron, the model 220, was an outboard sampler, with connections to a conventional oscilloscope as the readout display.

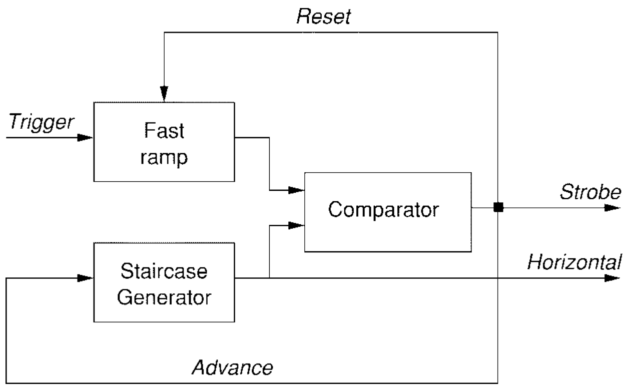


Fig. 3. Sequential sampling time base.

It was not long before the Hewlett-Packard Company (HP) and Tektronix Inc. got into the act. HP was first, with Tektronix Inc. following close behind . . ..

A. HP 185A

1960 brought Kennedy to office and the model 185A to HP. Carlson *et al.* [17] gave an overview of the 185A in 1959 at WESCON. The first *Hewlett-Packard Journal* of 1960 [18] devoted the entire issue to the 185A with a quote from Bill Hewlett stating:

> "The accompanying article describes what we believe to be a fundamental breakthrough in the field of high frequency oscilloscopes. The instrument. . . combines great bandwidth and high sensitivity with basic ease and simplicity of operation. It is in every sense of the word a general purpose instrument."

The 185A had a plug-in vertical amplifier and an internal time base. The first vertical amplifier, the model 187A, had a bandwidth of 500 MHz [18]. In two years, HP introduced the 187B with a bandwidth of 1000 MHz [19]. The 187 (both A and B) put the sampling gate in the probe since this was done in previous noncommercial instruments as described by McQueen (see Section I-A) and others. The sampling gate used the four-diode bridge; this switch had been known since at least Rad Lab days [20]. The diodes were matched to keep the bridge balanced.

The 187A introduced the use of a positive feedback loop to bring the charge on the sampling capacitor to input level, i.e., to bring the sampling efficiency to 100%. Since the time delay of the loop is small compared to the stretcher time, it is considered inconsequential. The gain of the loop could be varied by a control labeled "smoothing"; by reducing the gain, noise, and jitter in the system would be diminished. This feedback loop was described by Magleby and Van Duzer in a patent filed in 1959 [21]. An earlier patent on use of feedback with a four diode gate was filed by Stocker in 1953 [22]. It should be noted that feedback is not without problems: amplification after the sampling gate will amplify noise as well as signal. These problems will be addressed by subsequent designs.

Carlson described the time base circuitry of the 185A in a patent filed in 1960 [23]. His circuit includes improvements to reduce jitter and permit the use of time base "magnification." As shown in Fig. 3, the trigger fires a ramp; the ramp was compared with a staircase, then the sampling pulse was generated and the staircase was stepped. The staircase will be reset at the full-scale horizontal deflection. The comparator was designed to be precise and, therefore, reduce time base jitter. For waveforms with low repetition rates, the screen will be updated very slowly; therefore, Carlson devised another sweep circuit [24] to perform multiple samples per time point to accommodate rapidly changing waveforms.

The model 186A "switching time tester" [25] plug-in was introduced in March 1962. This system-in-a-plug-in included two bias supplies (0 to $\pm$30 V) and (0 to $\pm$10 V), a pulse generator (less than 1 ns) using step recovery diodes (SRDs) and a four-diode bridge sampling gate. The 186A was the first use of the newly developed SRD [26] in sampling literature.

Although tunnel diodes have largely faded from view, at this point, they were among the fastest diodes available. HP patented one design using back-to-back tunnel diodes [27] and a two-diode gate [28]. In 1964, Grove described the model 188A vertical amplifier with a 4-GHz bandwidth [29]. This novel amplifier featured several innovations including: 1) a feedthrough path suitable for time-domain reflectometry (TDR) [30]; 2) two separate input channels; and 3) an internal (i.e., not probe-based) sampler. The sampler itself was notable for being a two diode switch and was patented by Magleby and Grove [5]. A front panel control allowed restricted changes to the sampling diode biasing (by decreasing the pulsewidth), thereby *decreasing* sampling efficiency, but increasing bandwidth.

The sampler pulse generator used an avalanche transistor to create an initial pulse; this pulse was shortened by two-SRDs [26] and output to a shorted transmission line. The transmission line reflected the pulse back toward the generator and created a sampling pulse that is capacitively coupled to the sampling diodes. This classic design would be used many times by sampling gate designers.

B. Tektronix Model N and 661

The Tektronix model N was designed to plug into the 500 series oscilloscopes. It was notable for being an example of a "open cycle" (i.e., not feedback) system. The model N lacked a delay line, so the trigger had to arrive 45 ns before the signal or be delayed externally. A single diode was used as the gate (as in Sugarman's design in Section I-A) before being stretched, amplified and held in the "memory" capacitor. The timing unit would generate an "amnesia" pulse to reset the capacitor before the next sample was taken. Due to the design, input waveforms were limited to 120 mV.

The model 661 mainframe was introduced in 1963. Unlike the 185A, the 661 featured separate vertical amplifier and sweep plug-ins The vertical amplifiers (4S1, 4S2, 4S3) were feedback designs (like the 185A) and introduced the use of dc offset to the feedback loop. DC offset enables the user to effectively sample at a higher voltage level. The feedback loop of the 661 vertical amplifiers used a Miller integrator in the memory gate (called "rachet memory") that had low output impedance and improved accuracy [31].

The sweep units (5T1 and 5T3) offered both "equivalent time" and "real time" sampling. Tektronix Inc. was aware that

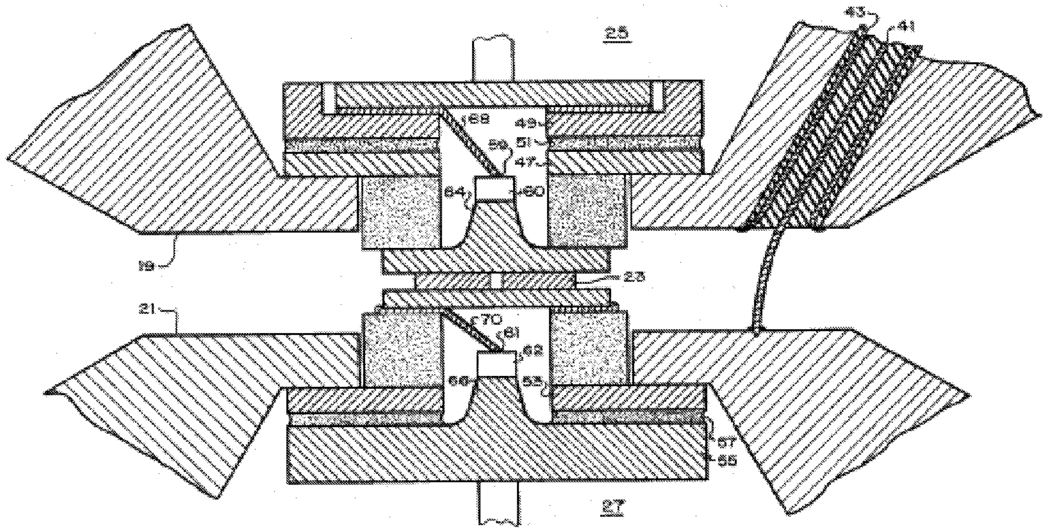


Fig. 4. Cutaway of Grove's two-diode sampling head from the patent [37].

sampling in real-time mode could exhibit beating with the input signal and, thus, they added a front panel control to modulate the sampling clock (by using the noise on the 60-Hz heater supply!).

The 4S2 dual-trace amplifier could be used with the P6038 sampling probe (patented in 1963 [32]). In the P6038, a differential amplifier was used to account for different ground potentials, as well as the feedback node for the closed sampling loop. Also notable was the use of a SRD [33] as the sampling pulse generator (concurrent with HP).

C. HP 140

In 1963, HP introduced the 140A oscilloscope system with both horizontal and vertical plug-ins. The sampling plug-ins were introduced in 1966 [34]. The sampling time-base came in two models, the 1424A single time base and 1425A dual time base with delayed sweep. The sweep circuits were described in two patents [35], [36]. The patents describe how to use a an additional timing ramp ("delay ramp") to measure the time after the trigger, as well as how to intensify the trigger on the screen. The vertical amplifier came in two basic models: the 1410A vertical amplifier (with both line inputs and probe inputs) and the 1411A vertical amplifier with an external sampler. The external samplers included the 1430A, 1431A, and 1432A.

The 1432A contained the same sampler as the 188A. The 1430A and 1431A were different models of the same new design. This new design set the standard for sampling until the new generation of monolithic sampling heads. Grove patented the design of the two diode sampling head in 1965 [37] (Fig. 4 shows the patent illustration: notice the injection of the pulse on the right-hand side). It featured a dielectric filled biconical cavity (Fig. 5 clearly shows the cavity, as well as the vertical diode mounting) with a thin coaxial pulse transmission line leading to the diode-to-diode connection. The sampling diodes were also special: they featured a very low chip capacitance (0.2 pF), low package inductance (250 pH), and the sampling

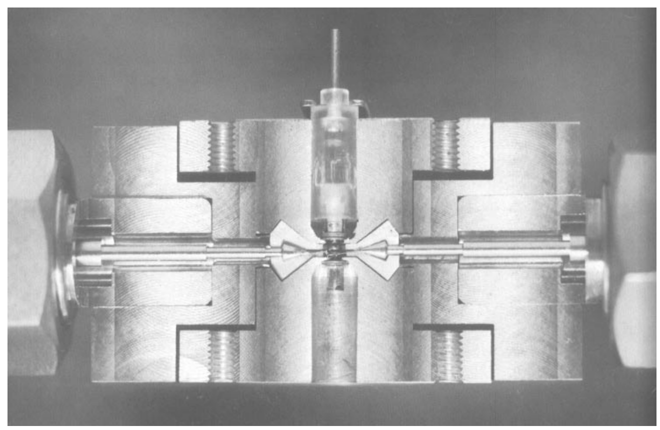


Fig. 5. Cut-through photograph of Grove's two-diode sampling head, from the October 1966 cover of the *Hewlett-Packard Journal* (©1966 Agilent Technologies Inc., Reproduced with permission, courtesy of Agilent Technologies Inc.).

capacitor was included in the package. The fast pulse was generated using the same shorted transmission-line idea as the earlier 188A, but, in this case, the pulse propagates via a biconical transmission line in the internal cavity. The resulting switching time was 28 ps (12.4 GHz). The only difference between the 1430A and 1431A samplers was the introduction of additional inductance in the cavity in the 1431A. The additional inductance forms a low-pass filter in combination with the diode capacitance and results in a lower voltage standing-wave ratio (VSWR), but at the cost of additional overshoot.

The two diode sampler was first analyzed by Best *et al.* in 1966 [38]. Another analysis was detailed by Grove in 1966 [39]. The 1430A was extensively studied by Riad before 1978 [40] and finished for journal publication in 1982 [41]. He disassembled a 1430A sampling head and measured the dimensions of the transmission lines, as well as the internal cavity. TDR was used to measure the parameters of the lumped parameters in the diode equivalent circuit. From these parameters, Riad was able to compute the step response of the sampling head in close agreement with the specifications published by Grove. Grove and Riad's model continues to find use as the primary model of the two diode sampling gate (see Section IV-B.3).

Interest in TDR was rapidly increasing following publication of Oliver's paper [30]. The 1415A TDR unit [42] was also introduced in 1963. It included a built-in 50-ps tunnel diode step generator. The 1415A used the same sampler as the earlier model 188A plug-in. The vertical axis was calibrated in ρ, the reflection coefficient[1] and the horizontal axis was calibrated in time and distance per unit time.

D. *Tektronix 1S Series*

After the 661, Tektronix designed two plug-ins for the 500 series oscilloscope mainframes. The 1S1 (introduced in 1965) was a single-channel sampler with a 40-ns delay line in front of the four diode sampling gate. It included a time base with a single time/division switch unlike the 5T3, which had two switches: one for real time and one for equivalent time. Triggering was done with tunnel diodes, which was novel at the time.

The 1S2 [43] (introduced in 1967) was a TDR unit, with two pulsers (1 V, 1 ns, and 0.25 V, 50 ps) and a horizontal calibration in either time or distance. Like the HP 1415A, the vertical axis could be adjusted for differing dielectric constants, specifically air, Teflon, or polyethylene. The sampling bridge on the 1S2 was the now familiar two diode bridge driven by the SRD and shorted transmission line. Now the response time of the 1S2 was up to the speed of the 188A and 1432A.

E. *Others*

Stuckert [44] (IBM) described a novel sampling gate constructed from two sampling bridges as part of a early computer-controlled oscilloscope system [45], [46]. The sampling pulse was delayed by differing amounts and, thus, the input gate would conduct while the second gate was shut off. Consequently, the first gate would shut off and the second gate would conduct, thereby isolating the input bridge.

F. *The 3 Series: 3S and 3T*

Responding to the 1430 series, Tektronix introduced the 3S series of vertical amplifiers and the 3T series of sweep units following the introduction of the 560 series of oscilloscope mainframes [47]. The 3S1 was a dual-channel vertical amplifier with a 1-GHz limit and external probes. With the 3S2, 3S5, and 3S6, Tektronix Inc. introduced the S series sampling head plug-ins (see Section II-F.1). The 3S5 and 3S6 were notable because the input channel gains were programmable by binary coded decimal (BCD) inputs: they were designed for use in an early automatic measurement system [48]. The 3S7 TDR sampler and 3T7 TDR sweep were essentially a two plug-in version of the 1S2 with the addition of a calibrated time–distance dial.

There were four different sweep units: the 3T2, 3T5, 3T6, and 3T77A. The 3T5 and 3T6 were, like the 35S and 3S6, designed for the R230 automatic test system and featured BCD programmable sweep speeds. The remotely programmable delays were implemented with a simple current digital-to-analog converter (DAC) controlling the delay circuitry. The 3T5 and 3T6 series switched to "real-time" mode when the sweep speed was low enough (less than 1 ms). The 3T77A was related to the 5T1A sweep unit and was conventional in design. However, the 3T2 sweep unit is truly notable for the introduction of "random sampling" (see Section II-F.2).

[1]The 1415A manual included transparent overlays for the screen that did crude conversion between ρ and complex impedance Z.

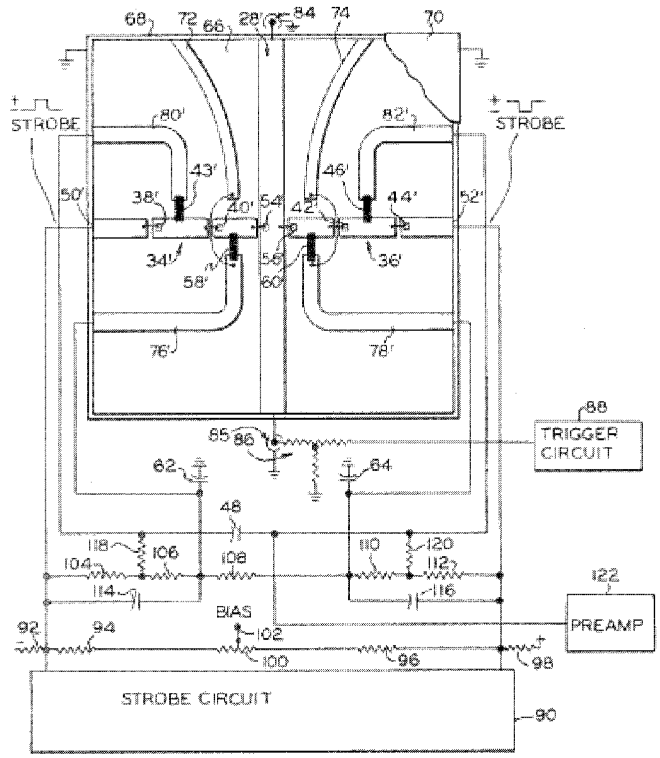


Fig. 6. Frye's traveling-wave sampling head (from the patent [50]).

1) S Series Sampling Heads: With the 3S2, Tektronix Inc. introduced the S series sampling heads. In total, Tektronix Inc. produced seven models of sampling heads and five miscellaneous heads (e.g., pulse generators and a trigger countdown). The S-1 and S-2 heads were simple two-diode samplers with bandwidths of 1 and 4 GHz, respectively. The S-3 was a four-diode probe unit with a 1-GHz bandwidth.

The S-4 [49], however, was different. This design featured the *traveling wave sampler* and was patented by Frye [50]. Instead of using the sampling pulse to positively bias the sampling diode, it used the trapped charge in the transmission line to switch the diodes. The advantage is that the switching time of the diode depends only on the fall time of the pulse generator and the time difference between two diodes (i.e., the transmission-line delay), not the pulsewidth of the pulse generator. Fig. 6 shows the construction of the head from the patent. This design was also used in S-6 head. The S-5 was also a traveling-wave design, but was built from discrete components instead of thick film and was designed for lower frequencies (less than 1 GHz).

In 1971, Andrews [51] described how to interface the HP 1430A sampling heads to the Tektronix 3S2 vertical amplifier. The most awkward part was the direct coaxial connection of the output from the 1430A into the 3S2.

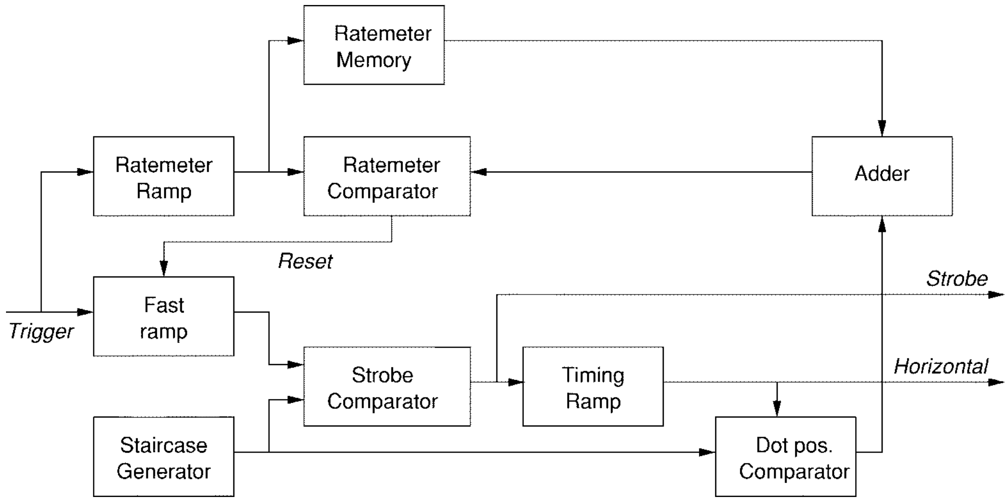


Fig. 7. Random-sampling block diagram.

Eventually frustrated by their inability to obtain 1430 samplers, Andrews and DeWitte [52] bought Merkelo's HP 5340A thin-film sampling gate (see Section III-C.1) from HP. This sampling mixer was used as the sampler for the Picosecond Pulse Labs S-1430D and S-1430E single- and dual-channel sampling heads. These heads were designed to be used with either the HP 140 or 180 series or as a Tektronix S series plug-in.

2) Random Sampling and the 3T2: Although one can treat McQueen's "anti-jitter" unit as a form of random sampling, the modern implementation and design dates back to Frye and Nahman's paper [53]. The basic idea, as they describe it, is to move the delay from the vertical amplifier input to the time base. It begins by triggering a timing ramp by the input waveform. The sampling pulse is *independent* of the input trigger. When the pulse is generated, the sample is taken and the ramp is stopped. At this point, the sweep is reset and a new input is awaited. Since the delay and input waveform are independent, the timing of the sample is "random" compared to a phase synchronous trigger unit. Therefore, this method has the advantage of avoiding the delay line required for synchronized sampling. On the other hand, the number of sweeps required can be substantial for slowly periodic waveforms.

Horñák's patents [54], [55] describe a sweep unit that encompasses both random and synchronized sweep. His randomized sweep is different from Frye and Nahman's conception because the horizontal position is derived from an asynchronous oscillator gated by the input pulse instead of a staircase.

The Tektronix 3T2 was novel since it made random sampling commercially available. The unit was designed to be used either with a conventional trigger or without a trigger. Fig. 7 shows the random sweep block diagram. As shown, the input trigger starts a downward timing ramp (called the "ratemeter ramp"); after a delay set by the "trigger ratemeter," it starts another downward ramp (called the "slewing ramp"); when it equals a downgoing staircase (time/division), then the sampling pulse is fired. Another comparator stops the ramp and thereby sets the horizontal position of the sample. A servo loop is constructed by comparing the output of the horizontal position (the stopped timing ramp) with the time/division staircase; this difference will be added into the delay of the trigger ratemeter. Without jitter, the error will be zero.

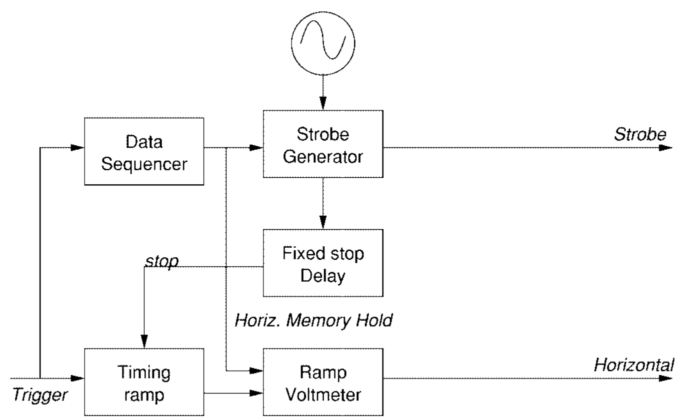


Fig. 8. Andrews' random-sampling time base [56], [57].

A novel random-sampling time base was designed by Andrews [56], [57] to measure high-speed switching waveforms from a low-repetition mercury switch. It was compatible with the 560 series oscilloscopes and, thus, is included here. It is most notable for having a "strobe predictor" with a random variation. The block diagram is shown in Fig. 8. As shown in this figure, the coincidence of the trigger and the free-running oscillator is used to measure the time interval. The probability of coincidence can be improved if the oscillator is phase locked to the trigger input. In the ideal case, the oscillator is locked and the result is a single dot. The voltage-controlled oscillator (VCO) can be intentionally jittered by addition of random noise generated by a reverse biased base–emitter junction. This design can be seen as the first step toward coherent sampling (see Section III-B).

Stuckert's CAOS system [45], [46] must be seen as the first truly computerized sampling oscilloscope. He used a Tektronix 564 storage mainframe with 3S2 and 3T2 plug-ins. The waveforms were digitized and then transmitted to a remote IBM model 360 computer mainframe.

G. 7000 Series and 180 Series

By the early 1970s, Tektronic Inc. and HP were focusing their efforts on the introduction of new oscilloscope mainframes and new plug-ins.[2]

1) Textronix 7000 Series: Tektronix Inc. continued refinements of the 3T2 when they introduced the 7000 series of oscilloscope mainframes. The 7T11 time base [59], [60] is a further refinement of the 3T2. Instead of measuring the ratemeter ramp against a staircase, it measures it against a constant limit; when that limit is reached, a separate "slewing ramp" is generated, which, in turn, generates the sampling pulse. This scheme reduces the jitter that would otherwise result from strobe delay.

The 7S12 TDR plug-in included a calibrated time base so that distance could be measured accurately. It required two S series plug-ins: one sampler and one pulse generator. The internal time base triggered the pulse generator and then reset the timing ramp. Like the HP 1415A (Section II-C), Tektronix Inc. also included an impedance overlay for the oscilloscope screen. The 7S14 plug-in was an interesting attempt to make sampling palatable to the nonsampling user; the "user interface" was nearly identical to a nonsampling oscilloscope.

2) HP 180 Series: HP introduced samplers for the 180 oscilloscope mainframe in 1971 [61]: the 1810A and 1811A vertical amplifiers, the 1815A and 1818A TDR units, and the 1821A time base. Like the Tektronix 7S14, the 1810A vertical amplifier attempted to make the user interface simpler by elimination of the smoothing control and design of oscilloscope-like triggering. The 1811A used the same Grove samplers (see Section II-C). HP provided two TDR units: the 1815A TDR plug-in has an outboard sampler (the model 1817A) with one 1430A sampler and one slow-speed pulser (a tunnel diode mount), whereas the model 1818A had a 170-ps pulser built in.

III. Technology Improvement

Unheralded technological improvements are constantly made that may or may not find their way into commercial products. The following sections review specific technologies developed before the introduction of integrated sampling gates.

A. Transient Sampling

Previously, we have assumed the input signal is repetitive or periodic in nature. However, certain waveforms, like the output of radiation detectors from nuclear explosions, only occur once. If the waveform can sampled at multiple points in time simultaneously, then it should be possible to sequentially display each sample.

Kerns' patent [62] proposed using multiple samplers at regular points along a transmission line (e.g., cable) output to sample-and-holds, which were displayed sequentially. Espenlaub and Leotta [63] essentially describe the same concept specifically for a coaxial transmission line. Schwarte [64] also discusses a 40-tap delay line with 40 two-diode gates. Bernet and Lejeune [65] used multiple samplers connected to a single input point. The output of the samplers were connected to charge-coupled device (CCD) delay lines; the samplers were strobed in an interleaved fashion. Buchele [66] described a fast-in slow-out (FISO) sampling system with the same tapped delay line, but with more modern A/D converters. Conway *et al.* [67] implemented a microwave receiver with a switched tunable filter before the meandering transmission line as an option, as well as discuss the use of undersampling to downsample the input waveform. McEwan [68], [69] updates the technology, but the concept is identical to Kerns original invention.

Jenq [70] discusses the spectral effects of nonuniformly sampling a signal along a delay line. He also proposed a digital signal processing (DSP) solution [71] to correction of interleaved samplers by applying adjustable delays.

An optical approach was taken by EG&G [72]. They converted the electrical pulse into a light pulse via a laser. The light pulse was transmitted down an optical transmission line (Kerr cell) that was sampled at multiple points by samplers; each one was digitized by an A/D converter.

B. Time-Base Design

Time-base (sweep) circuits are either *equivalent time* or *real time*. In the *real-time* mode, the sampling strobes occur at fixed intervals after the trigger. There is only one trigger per sweep, as opposed to equivalent time sampling. In equivalent time, each triggers enables a variable delay: in the *sequential* mode, this delay is increased by a constant amount at each trigger until the end of the sweep. In the *random* mode, the delay between adjacent samples is not constant. In the *coherent* mode, a sampling clock is locked to the incoming trigger frequency.

1) Jitter and Drift: As alluded to earlier, the precision of the time base (including jitter and long-term drift) is also important to the design of the sampler. Jitter in the time base results in sampling the input waveform at the wrong time and, therefore, in the wrong place. Jitter is a short time phenomenon often resulting from noise. Drift is a long-term phenomenon resulting from many causes, particularly temperature dependencies in the timing circuits.

Lüscher [73] described a time base with low trigger delay (20 ns) and low jitter using tunnel diodes and transistor current switches. The time base was good to approximately 5 GHz. Uchida *et al.* [74] (Iwatsu) used a "flywheel" circuit to maintain synchronization over blanking intervals. A related patent by the same group [75] automatically synchronizes the input waveform by amplifying (or attenuating) the input to the sync circuit depending on the derivative of the input waveform. Since nonlinearity in the timing ramp effects jitter, Toda *et al.* proposed adding a correction lookup table before the step generator DAC.

Elliot [76] compensated for drift by employing a lock-in amplifier [77] to adjust the horizontal position (time base) by locking to a fixed frequency. Improving horizontal position also improved the vertical resolution as well.

2) Coherent Sampling: In random sampling, the "Missing Waveform Phenomena" [78] is due to the varying and nonrational relationship between the sampling clock frequency and input frequency. The missing waveform phenomena can be ameliorated by the addition of pseudorandom noise [79]–[81] (also, see Andrews' time base in Section II-F.2) to the sampling clock, but long acquisition times may result before the clock phase

[2] Addis [58] tells the story of the Tektronix 7000 series versus the HP 180 series; it makes for an amusing and cautionary tale.

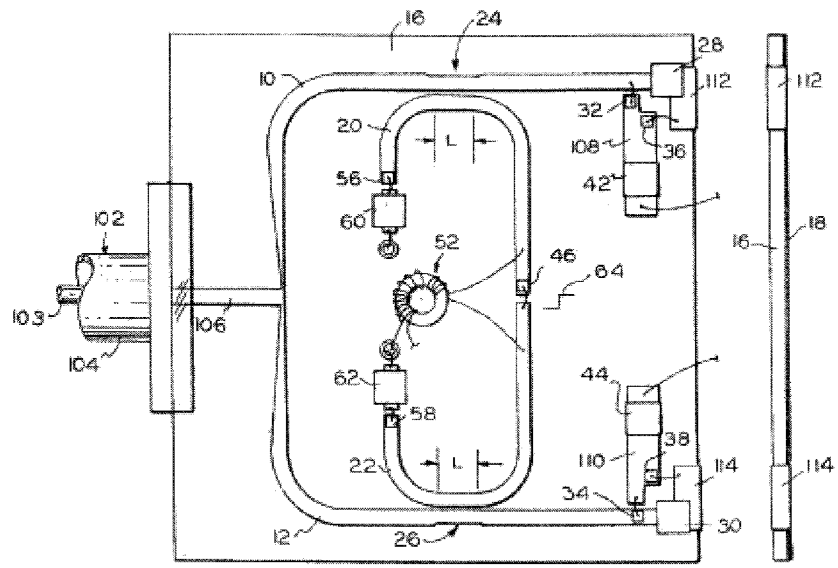


Fig. 9. Lockwood's sampling gate (from the patent [91]).

is randomized. In one method of coherent sampling, the sampling clock is generated by a phase-locked loop with a VCO. At Tektronix Inc., Agoston [82] used a microprocessor to modify the strobe timing by programming a DAC with a frequency offset (to the VCO). The microprocessor also controlled a time measurement section and triggering. Earlier, he also used a microprocessor to perform pseudorandom sampling by interval measurement [83]. A similar idea used a time base to phase lock an oscillator to the input waveform [84] so that, by proper choice of the loop bandwidth, jitter would be reduced. The Microwave Transition Analyzer [85], [86] used fast Fourier transform (FFT)-based analysis of the IF waveform (after the sampler) to adjust the frequency of the sampling clock oscillator.

3) Other Time-Base Developments: Nakaya [87] described how to do time-base "magnification" for a triggered sampling time base by changing the sweep waveform. Best's earlier patent [35] magnified by using a second "delayed sweep," as mentioned in Section II-A. A related patent by Soma and Kohno [88] describes automatic adjustment of the trigger delay by finding waveform peaks.

C. Sampling Circuit Improvement

Since sampling gates are one of the most critical parts of a sampling system, there had been considerable time and effort spent on improving the technology behind these circuits. In addition to improving switching times, correcting for lower sampling efficiency during slow repetition rates is also a concern. Also, since strobe kickout (feedthrough of the sampling strobe through the gate to the input) and blowby (the transmission of high frequencies through the open sampling gate due to the capacitance of the sampling diodes) can also effect the charge on the sampling gate capacitor, effort has also been expended on reducing the effect through careful circuit design.

1) Sampling Gate Technology: Merkelo [89], [90] described the design of a thin-film sampling head. Essentially, it is a technological update of Grove's sampler—the diodes were beam lead (low inductance) connected to a slotline. The voltage standing-wave ratio (VSWR) was only 1.7 over a broad frequency range.

Lockwood [91] further modernized the sampling gate by introducing transmission-line construction including directional couplers for the trigger pickoff and pulse injection. This construction is clearly seen from a patent figure (Fig. 9). The use of directional couplers for pulse injection reduced kickout. This design was further improved by using a shorted slotline to reflect pulses generated by the SRD pulse generator and a coplanar waveguide [92]. Axell [93] described a very similar sampler.

The HP 5356A/B/C counter sampling heads [94] used an update of Merkelo's sampler (see Section III-C.1) to implement a harmonic heterodyne counter. The new sampler used a thin-film hybrid that included a two-diode GaAs sampling gate chip together with a SRD pulse generator. This design was fully integrated into GaAs by Gibson [95] for the HP 5350/1/2A counter.

Prevot [96] described a two-diode waveguide sampler that includes the pulse diode at the end of the waveguide. One problem with this arrangement is the impedance mismatch of the waveguide-to-coaxial transition.

2) Gate Circuit Design: Sampling bridges must be turned off precisely (symmetrically) by removing the bias on the two bridge midpoints. Benson described a four-diode sampling bridge with a feedback loop that balances the dc offset and turns off all diodes together [97]. Gloaguen [98] described a modification with a single switch for both branches of a two diode gate. Uchida [99] proposed a number of small changes to the basic four diode gate to: 1) better match the pulse generator VSWR and 2) reduce blowby by changing circuit time constants.

One can also use the modern day equivalent (FETs) of the earliest sampling gates (pentodes). Due to their high impedance, FETs can offer better isolation from the input when switched off. However, the gate capacitance can be problematic because of kick-out and blowby. Liechti [100] first described the use of a dual-gate GaAs MESFET as a pulsed amplitude modulator.

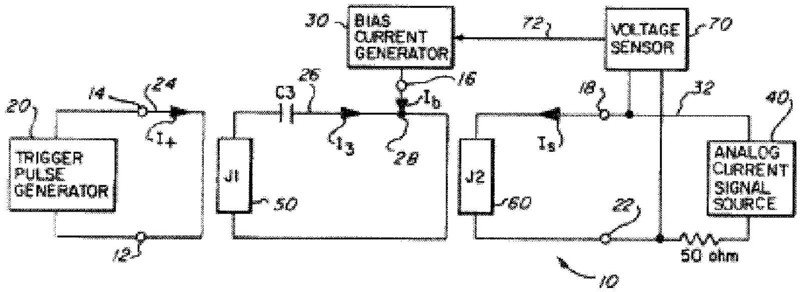


Fig. 10. Hamilton's sampling gate (from the patent [127]).

Akers and Vilar [101] constructed a dual-gate MOSFET sampling gate good to 9.4 GHz. A single-gate MESFET was used by Hafdallah *et al.* [102] to construct a sampling gate good to 2.4 GHz. A further study [103] compared the step response of a large-signal MESFET model with the measured results [104]. One can also use MESFET nonlinearity for pulse shaping [105]. The latest result [106] combined the pulse shaping of the nonlinear transmission line (NLTL) (see Section IV-A.1) together the earlier sampler to demonstrate a hybrid MESFET sampler with a 28-ps resolution.

Heterojunction technology can also be used to construct high-speed sampling gates. LeCroy experimented with this technology circa 1994 [107] and achieved high speed (10 GHz) together with good linearity.

Differential samplers [108] find use in TDR as well as network analysis. McEwan combined a differential sampler [109] with a resistive bridge to create a directional sampler, e.g., a sampler and directional coupler. A fully integrated version will be discussed in Section IV-A.1.

3) Stretcher Improvement: Another approach to increasing sampling efficiency is to take more samples per dot. Such an approach was originally proposed by Carlson [24] and was again outlined by Hansen [110]. In another way to increase the sampling efficiency, Frye [111] introduced a capacitively coupled feedback loop after the input sampling gate. He also introduced a resistive feedback loop after the memory gate to increase dc stability for low-repetition rates.

Nakaya *et al.* [112] addressed problems of droop in the memory (stretcher), as well as noise produced by the gain after the sampling gate by using additional feedback paths in the vertical amplifier.

4) Blowby Compensation: Metz [113] proposed the use of a balancing bridge after the sampling bridge to minimize strobe feedthrough and decrease blowby. Agoston [114] addressed blowby compensation by using a current steering network to charge the capacitor. Another approach is to add a feedforward frequency compensation network [115] to correct for distortion.

The traveling-wave sampler [49] (see Section II-F.1) used in the Tektronix S-4, S-5, and S-6 samplers has two problems: first, the sampling pulse must be large enough to turn on all of the reverse-biased sampling diodes; this also limits the dynamic range of the input signal. Second, blowby effects the trapped charge in the delay line of the sampler. Agoston [116] modified the traveling-wave sampler to include a microcontroller that digitizes the output of the track and hold (i.e., stretcher) and digitally controls the gate bias. Chang [117] provided the first analysis and simulation of the traveling-wave sampler in his Ph.D. dissertation. His experimental sampler was operational to 26 GHz. Thomann *et al.* [118] proposed using the traveling-wave gate, but with corrections for the blowby distortion, and claimed a 21-GHz bandwidth with discrete components.

5) Kickout Reduction: Since strobe kickout can also effect the hold capacitor, Bosselaers [119] isolated the sampling diodes from the sampling pulse by coupling the pulse via a balun and then increased the dynamic range and simultaneously sampling efficiency by using a traveling-wave gate, much in the manner of Frye (see Section II-F.1).

Dobos and Metz [120] used a unity buffer amplifier as an isolator in front of the sampling bridge followed by a differential amplifier to accommodate changes in ground potential. Madani and Aitchison [121] described a sampling hybrid good to 20 GHz. Like Dobos and Metz, they used an amplifier before the sampling diode pair as an isolator; this prevents kick-out as well as improved VSWR. Careful design produced fairly flat spectrum. Most recently, Goumaz [122] describes a sampler with a common base transistor switch as an isolator, followed by a charge amplifier and current-to-voltage conversion.

6) Nonlinearity Correction: Browning [123] proposed using multiple point sampling (just as Carlson [24] did earlier as well as Hansen [110]) as well as digitizing with an A/D and matching multiplying D/A in the feedback loop.

Bilterijst [124] (Philips) attacked the problem of maintaining a balanced charge by using a symmetric microstrip transmission line as a distributed capacitor rather than a discrete capacitor. The patent also described improvements to the SRD pulse generator to improve the symmetry of the pulse.

HP also used a A/D $\rightarrow$ D/A circuit in the 54 120 sampling oscilloscope [125]. They introduced a memory between the two converters to correct for nonlinearity in the sampler transfer function.

7) Josephson Junctions: The extremely fast switching time and low noise of Josephson junctions led to their use in sampling (the cyrogenic temperatures are also beneficial to time-base jitter and drift). A Josephson junction sampler was first described by Hamilton *et al.* [126] and subsequently filed as a patent [127]. They recorded a time resolution of 9 ps, but was not capable of measuring arbitrary waveforms. A block diagram from the patent is shown in Fig. 10, with the Josephson junctions shown as $J1$ and $J2$. Concurrently with Hamilton, Faris of IBM was also building a sampling circuit [128] that adjusted bias and pulse timing to scan the input waveform (Faris filed later the same year [129], [130]). Time resolution as low as 2.1 ps was reported by Wolf [131]. Kobayashi and Tazoh (Iwatsu) also filed a patent for an improved version of Hamilton's sampling gate shortly after Faris [132].

There are at least two difficulties with Josephson junction samplers: first, the dynamic range is limited by flux quantization inside the loop; second, the transition back into the superconducting state at the sample point. Sage *et al.* described two different circuit modifications that produced a 10-GHz 6-bit sampler.

Bodin *et al.* [133] describe in great detail the construction of a 5.6-ps experimental sampling system including details of the flip-chip bonding.

A detailed analysis of the Josephson junction sampling gate was done by Van Zeghbroeck [134], who pointed out fundamental tradeoffs between speed and accuracy. A simultaneous paper was published by Wolf [131]. A related study of the effect of pulsed Josephson junctions was done by Kratz [135]. He compared simulation with the equations and found good agreement in a proposed sampling gate.

The commercialization of Josephson junctions technology was done by Hypres Inc. They obtained an 8-ps risetime using a silica substrate with a corner cooled by the liquid Helium flow [136]. Whiteley's patent [137] included numerous circuit details. Other patents, filed by Hypres [138], [139] described the TDR circuitry details.

New high T_c materials led to a 120-GHz sampler [140], [141]–[143] operating at 40 K to be used in measuring 40-Gb/s waveforms. A notable achievement is the measurement of the device-under-test (DUT) operating at room temperature.

D. Dual Samplers

In systems that require dual samplers (such as network analyzers or two channel TDRs), there is a potential for phase mismatch between the channels. Furthermore, in a sampling frequency converter, the SRD may require 4–5 W of power. One solution to these problems is the use of a power amplifier *per channel* rather than use a lossy power splitter. To limit the phase shift, a temperature compensation circuit can be used. Both of these methods were described in a Wiltron patent [144]. Agoston *et al.* [145] proposed a different approach to a dual-channel TDR: use a single SRD and a coplanar waveguide; a waveguide coupler is used for each channel.

E. Optical Strobing

One alternative to using electrical switching of sampling gates is the use of optical pulses. Andrews and Lawton [146]–[149] described a dual-channel sampling head (compatible with the HP 1411A vertical amplifier) that used a bulk GaAs semiconductor as the photoconductor and a laser diode as the stobe. There are two principal advantages to using a photoconductive sampling gate: first, since the strobe is optical, kickout is eliminated; second, dynamic range is greatly increased since diode breakdown is not an issue.

IV. Integrated (Monolithic) Gates and Computer Interfaces

Grove's 1430 sampler (see Section II-C) can be seen as the last step in sampling gate development before the wide-scale introduction of custom integrated circuits. Merkelo's thin-film gate (see Section III-C.1) marked the beginning of a new era for sampling gate-based instrumentation since it depended on precise thin-film technology. Frye's earlier S-4 traveling-wave sampler (see Section II-F.1) used thick-film technology on a ceramic substrate.

The 1990s can also be seen as the introduction of computer technology to all aspects of sampling measurements from control of the sampling gates to time bases and use of measurements.

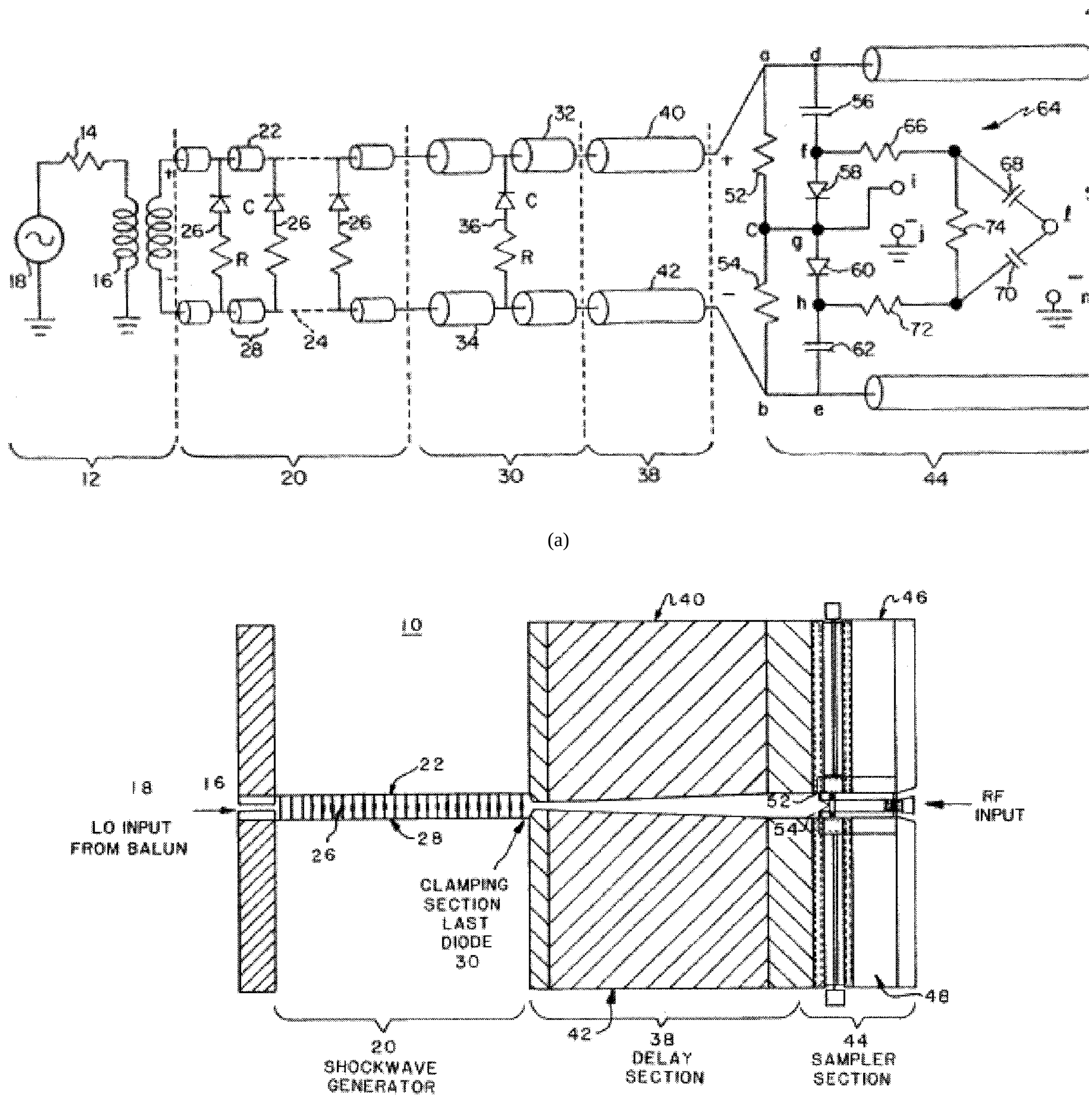
A. Sampling Heads—Monolithic Samplers

The rapid advancement of semiconductor technology led to the inevitable construction of monolithic samplers. Further development of process technology enabled the construction of combined RF and optical circuits.

1) NLTLs: NLTLs were described in 1960 by Landauer [150], [151] at IBM, and later by Jäger [152], [153]. However, the NLTL was not really brought to fruition until the work by Rodwell *et al.* [154]. They built a 20 : 1 scale model using 45 discrete diodes; the resulting NLTL compressed a 525-ps fall time to 100 ps. This design is further described in a related patent [155] and Rodwell's dissertation [156]. All the steps necessary to design and fabricate an NLTL in GaAs are given in a patent by Bloom's group at Stanford University [157]. By careful scaling of the devices in the NLTL, the input and output impedances can also be made to match without a transformer [158]. These NLTLs are typically made using Schottky diodes as variable capacitance elements. However, they sharpen the pulse only on the falling edge. If the circuit is designed using antiparallel diode pairs [159], then both edges can be sharpened.

Su *et al.* of HP patented a completely integrated sampler [160] that included an integrated NLTL [161] and a two-diode sampling gate. The NLTL was implemented using a series of varactors. However, this presented a number of problems, most notably, turn-on time, diode nonlinearity, and mismatched impedances. A subsequent patent [162] described how to choose the diode values to accommodate these design problems. Whiteley *et al.* [163] described the complete sampler hybrid circuit including the SRD pulser, balun, and NLTL enhanced sampler (shown in Fig. 11). This borrows heavily from the Stanford group and Rodwell's dissertation [156] work in particular.

The sampling gate design combined with the NLTL was described in patents [164], [165], as well as a paper [166]. Later, Rodwell and his group used Schottky diodes as nonlinear shapers as part of a monolithic GaAs circuit that generates extremely fast pulses for millimeter-wave sampling [167], [168]. His group also developed a simpler three-mask GaAs sampler using the NLTL [169]. In this design, a 30-ps pulse was compressed to 2 pis by the NLTL. This pulse is then injected to a coplanar waveguide, which fed the two sampling diodes. This design was used as part of a TDR unit for use



(a)

(b)

Fig. 11. HP's sampler (figures from the patent [163]). The circuit is shown at the top, the mask layout on the bottom. It includes a balun (12), NLTL pulse sharpener ("shockline," 20), clamping section (30), and sampler section (44).

in time-domain network analysis [170]. Rodwell's group also achieved a fall time of 680 fs (725 GHz) by using elevated coplanar transmission lines and reduction of parasitics [171].

Marsland [172] points out the shortcomings in the HP 8510 Network Analyzer Wheatstone bridge [173], particularly the difficulty in constructing a wide-band bridge. Also, since the sampling gate was not floating, it had to be connected to a balun. Marsland then described how to design and fabricate a two-gate floating directional bridge. This patent is very complete and includes fabrication recipes. However, the directionality was limited by the resistor fabrication. The use of integrated directional couplers and the NLTL was used in a frequency-domain network analyzer [174].

Using an NLTL and a directional sampling bridge, Yu *et al.* [170] designed and fabbed a monolithic TDR chip that exhibited a 2.3-ps fall time for use in a time-domain network analyzer [175]. This circuit was mounted directly on the wafer probe using small probe tips. Fig. 12 shows a newer design [176] using a micromachined probe tip. Shakouri *et al.* measured a 880-fs fall time (500 GHz) with this apparatus. van der Weide [177] reported a 480-fs fall time measured by an on-chip sampler at room temperature in 1994.

An interesting example of the application of the NLTL is the combination of a Schottky photodiode with a sampler. Rodwell's group [178] and the Stanford group [179] designed these circuits to measure very fast laser pulses.

2) Resonant Tunneling Diodes (RTDs): RTDs have less jitter than other triggering methods and have been shown to have extremely fast rise times and triggering (up to 110 GHz) [180], [181]. Instead of using an SRD with an NLTL, another sampling head integrated circuit was fabricated using RTDs [182], [183] in place of the SRD. The bandwidth was calculated to be 26 GHz. A recent realization used RTDs at the top and bottom of a four-diode bridge [184].

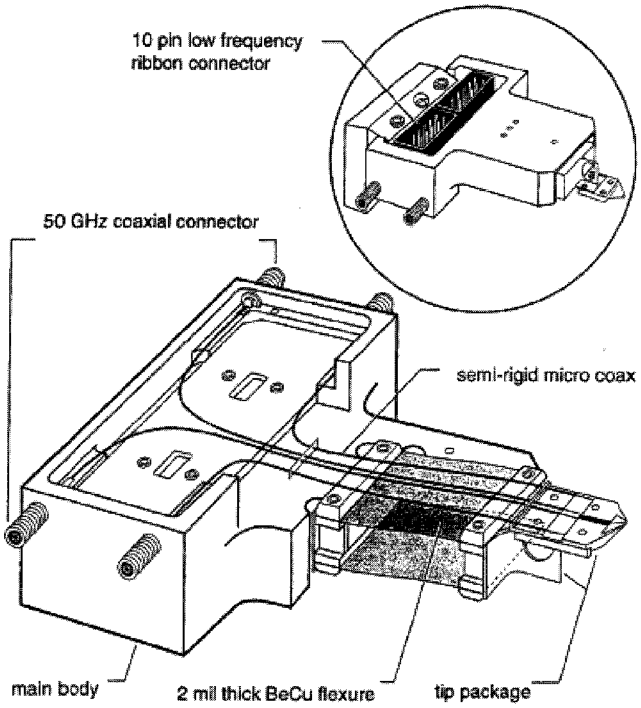


Fig. 12. Bottom view of a 500-GHz wafer probe with sampler and micromachined tip (reprinted with permission from [176]).

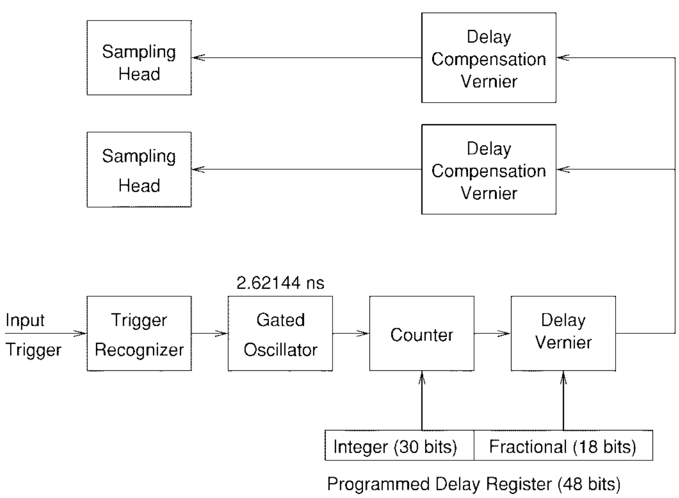


Fig. 13. Time base of the Tektronix 11801B [186].

B. Digital and Computer Control

The introduction of digital technology improved many aspects of sampling functionality, as well as providing conceptually simpler designs. Unfortunately, the detailed design concepts and algorithms are not publicly available. Modern computer control has enabled more accurate time bases, as well as sampling gate characterization and compensation.

1) Time-Base Design: Dobos [185] first described measurements of the time base for the Tektronix model 11 801 digitizing sampling oscilloscope. A further description [186] gives more details on the design, shown in Fig. 13. Like the locked oscillator schemes mentioned earlier (see Section III-B), the time base used a triggered VCO [187] as the source of timing. The output of the oscillator serves as the clock for a pre-loaded 30-bit counter acting as the integer part of a delay. A separate 18-bit register serves as the fractional part. This digital design is more precise than the timing ramps used in the earlier time bases.

Coherent sampling (see Section III-B.2) can be obtained when the ratio of input frequency to the sampling frequency are relatively prime. The problem is how to adjust the sampling frequency to *closely approximate* being relatively prime. Reynolds and Slizynski [188] propose searching Farey series to find an optimal ratio. Kimura *et al.* [189] present a simpler mechanism for finding a relatively prime time interval. The implementation was described in great detail in patents by Uchida and Kobayashi [190]–[192].

2) Time-Base Correction: Distortion resulting from time-base error (including jitter) can be corrected if the time base can be characterized. Jitter limits the input bandwidth, therefore, compensation will produce a wider measurement bandwidth [193], [194]. An early study of this error was done by Gans [195]. He was able to deconvolve the probability density function of the sampling jitter from the input waveform. One approach to drift compensation is to process the waveform in the frequency domain and apply an inverse phase shift and transform back [196]. Time-base nonlinearity can be characterized or measured with a sine input and comparing the expected zero crossings with the measured crossings. A spline function can then interpolate the points and correct for nonlinearity [197].

Shinagawa *et al.* [198] provides an early model for separating signal source jitter from sampling gate jitter. Souders *et al.* [199] examined the bias resulting from time-base jitter with monotonic waveforms. They proposed both a median and Markov estimation method for jitter characterization. Verspecht [200] further extended Gans work by easing restrictions on waveform shape and analyzing the effects of additive noise. He further examined the effect of phase errors resulting from errors in the timing of the sampling pulse [201]. Phase demodulation of the sine input together with windowing, can produce accurate measurements of time-base distortion [202], [204]. However, windowing also produces discontinuities in the corrected output. Many of these results are discussed in his dissertation [204].

Another method proposed uses a pure sine tone as input and then calculates the fit against the measured output [205]. This assumes a perfect time base, so Pintelon and Schoukens [206] presented one method to compensate for distortion due to “systematic errors” in the time base (as opposed to jitter). Stenbakken and Deyst [207] compared the various approaches; later they described an iterative sine-fitting method [208] that accommodates harmonics and noise. More recently, Wang *et al.* [209] described a different least-squares approach. Vandersteen and Pintelon [210] show that maximum likelihood (ML) estimators are just as effective. The ML estimator was compared against earlier methods and the results clearly illustrate varying time-base distortion, as well as the robustness in spite of nonlinearities. More recently, Kobayashi *et al.* [211] analyzed and measured the effects of jitter and the finite aperture on signal-to-noise ratio in a sampling gate system.

3) Calibration and Characterization: Another example of computer use is for calibration and characterization of samplers. Riad’s early work (see Section II-C) was devoted to detailed

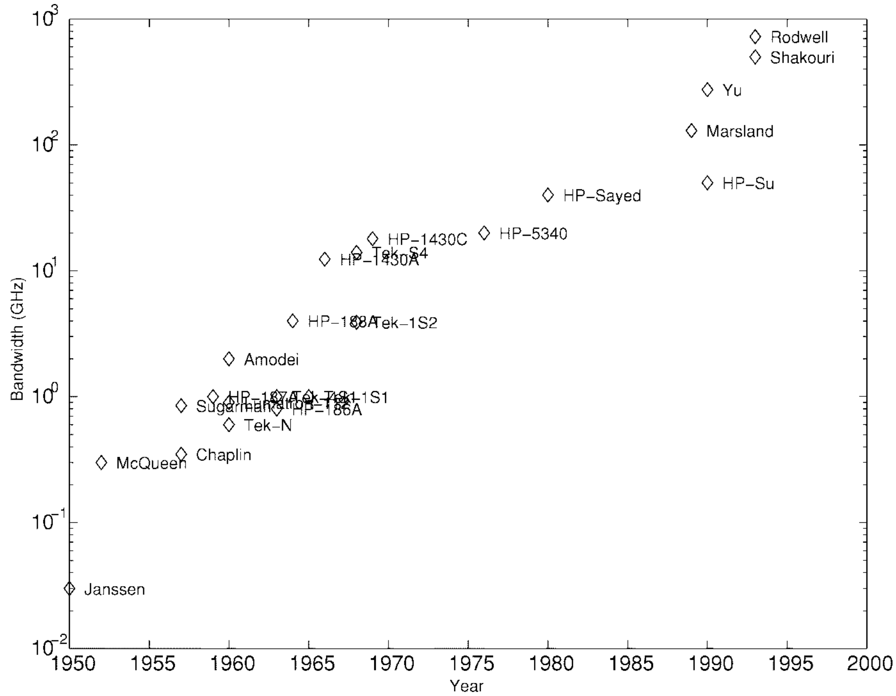


Fig. 14. Time line of sampler development.

modeling of the 1430 sampling gate so it could be deconvolved from the digitized waveform. Further work on deconvolution was motivated by measurement noise and other computational difficulties since inversion of the convolution of the input signal with the gate impulse response can be considered an "ill-posed problem" particularly when the signal is contaminated by noise.

Guillaume and Nahman [212] explored the use of the Fourier transform for deconvolution under experimental conditions and studied the use of filters for noise elimination. One of Riad's students studied the design of an optimal compensator that minimizes error energy and limits noise [213]. Riad [214] conducted an overview of deconvolution circa 1985; another of his students (Bennia) described how to perform a filter design optimization to reduce noise and the resulting computational difficulties [215]. Bennia and Nahman [216] modified Guillaume and Nahman's method to ensure a causal filter. This work was further extended to combine the best features of the Guillaume–Nahman method with the Bennia–Riad iteration method [217]. A noniterative approach to filter optimization together with analytic reconstruction filtering for deconvolution was recently proposed [218], [221].

Another approach is to model the sampling gate as a discrete time system and then apply system identification [220]. For weakly nonlinear systems, a truncated Volterra series can be used to model the transfer characteristics of a sampling oscilloscope [221]. After finding the Volterra kernels, a compensation procedure can be applied.

Of course, compensation methods are only good when the model is well characterized. As the gates get smaller, characterization becomes more difficult. Rush and his colleagues [222] realized that the kickout of the sampling pulse would represent a good way to characterize the sampler. Further work by Verspecht and Rush [223], [225] detailed the procedure and compared it against measurement and theory.

Additionally, the interconnection network between the sampling diodes and the inputs can be analyzed and the modeling error can be shown to be bounded and small [226]. Riad's model of Grove's two-diode sampler (see Section II-C) can be extended to include the strobe pulse generator impedance, diode imbalance, and nonlinear diode capacitance [227]. This model has been taken further: the nonlinear diode junction capacitance can produce an error, even in the nose-to-nose calibration [228]. Further, modeling the time-varying junction capacitance is not sufficient to capture all of the error seen in nose-to-nose calibration [229]. Despite these nonlinearities, the nose-to-nose calibration method (and normalization) can be shown to have good agreement with swept sine methods [230]. A detailed study of the effect of offset voltage showed that bandwidth limitations occur when the offset is too large [231].

V. Previous Reviews

The earliest review of sampling oscilloscopes formed a section in a book on short pulse measurements [232]. A very early journal paper [233] featured a comparison of an experimental IBM sampling oscilloscope [15] and the Lumatron models and the Tektronix Type N. A book published in the former East Germany and translated and reprinted in the west also covered sampling oscillography as part of a chapter on testing [234]. An early review by Tektronix Inc. [235] covered the Type N and the model 661. Tektronix Inc. described their sampling technology circa 1970 [236] in a compendium of sampling circuits from various models dating back to the 1S1.

Nahman [237] reviewed subnanosecond pulse measurement technology circa 1967. His paper included looks at other nonsampling-based measurement techniques including real-time oscillography. He updated his paper three more times [238]–[240]. His last review included extensive mention of electrooptical methods. Concurrently, he also reviewed and compared the state of deconvolution [241].

Riad [243] gave a short overview of sampling including various gates and their implementation in various sampling oscilloscopes. In a more modern and comprehensive review, Cochrane [244], [245] surveyed both the theoretical and practical aspects of sampling technology circa 1989.

Rodwell and his group [246] reviewed the use of NLTLs in various applications including sampling (as discussed in Section IV-A.1). Marsland *et al.* published an overview on the use of NLTLs in instrumentation circa 1990 [247]. The use of sampling and other methods in wafer probing was reviewed by Schumacher and Strid in 1990 [245].

Andrews [249] reviewed the state-of-the-art of sampling oscilloscopes by using a single pulse generator to compare the output of different manufacturers. He found variations in the waveforms sampled by these different systems. More recent tests [250]–[253] continued to find differences. A round-robin test conducted by NIST in 1997 [254] revealed that, although the initial transient was adequately represented, the settling period (2 ns after the transition) differed from manufacturer to manufacturer.

Henderson *et al.* [256] reviewed the nose-to-nose calibration method and also their electrooptic calibration apparatus [257]. They found remarkable agreement between the two methods. A third method, using a stepped frequency measurement, demonstrated considerable agreement.

A fascinating overview of the Soviet (now Russian) sampling technology can be found in a review by Ryabinin *et al.* [258]. They discuss the features of eight different sampling oscilloscopes, as well as corrections for "infiltration" (blowby). Ryabinin's book [259] is unknown in the west, but it is truly remarkable for its scope and theoretical detail.

VI. Conclusion

For low-frequency microwave signals, fast A/D converters have replaced the use of samplers (particularly in digital oscilloscopes). However, there is nothing quite like a sampler for high (currently as high as 60 GHz for commercially available oscilloscopes) input frequencies.

Fig. 14 illustrates the progression of samplers over the last 50 and more years.

The past 50 years have seen an incredible advancement of microwave, semiconductor, and computer technology. The history of RF sampling reflects this advancement and achievement.

Acknowledgment

This paper would not have been possible without the interest of S. F. Adam (formerly of the HP Microwave Laboratory, Palo Alto, CA) over 30 years ago. The kindness of L. Renihan (also formerly of HP Microwave Laboratory) is also remembered. The tolerance of the entire HP Microwave Laboratory (5U, Palo Alto, CA) at the time is also appreciated. R. Hager, R. C. Melville, and J. J. Larkin have been enthusiastic supporters of the author's sampling habit. N. Moayeri and D. DiGiacomo helped with paper preparation.

The encouragement and comments of J. R. Andrews, Picosecond Pulse Laboratories, Boulder, CO, enriched this paper considerably. This TRANSACTIONS' Editor-in-Chief D. Rutledge, California Institute of Technology, Pasadena, and former Associate Editor R. York, University of California at Santa Barbara, helped with the final submission of this paper; additionally, the referees offered many helpful comments and suggestions.

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